White Paper

Transient Behaviour Of A Power MOSFET

Mounted On A Heat Sink

Report number : R2013-053
Revision : 2.0
Date : 16 April 2014
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Abstract

This paper discusses the impact of transient behaviour of a semiconductor on the selection of the thermal management solution. An application with a MOSFET mounted on a heat sink is evaluated for both steady state and transient behaviour. The thermal management solution based on the average power dissipation will lead to the FET exceeding its junction temperature limit. The paper show the benefit of using electrical network analyses tools to solve transient thermal problems. And using the analyses to selection an optimal cooling solution.

Revision History

Version	Date	Remarks
1.0	4 June 2013	Initial release
2.0	16 April 2014	Reformatted and general revision of the white paper

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Nomenclature

C	Thermal capacitance in J/K
H	Height, mm
h	Heat transfer coefficient, W/m²·K
h'	Thermal impedance, K·m²/W
h'	Thermal impedance,°C·cm²/W
F	Force, N
I	Current, A
k	Thermal conductivity. W/m·K
L	Length, mm
m	Mass, kg, grams
p	Pressure, Pa
p	Pressure, psi
P	Power, W
$\dot{Q}$	Heat transfer rate
R	Thermal resistance, K/W
T	Temperature, ºC or K
t	Time in seconds, milliseconds
W	Width, mm

Subscripts

amb	Ambient

Abbreviations

DC	Duty Cycle
HS	Heat Sink
TIM	Thermal Interface Material

1 Introduction

A power MOSFET used with pulsed power dissipation can fail if the thermal design is only based on average power dissipation. This paper will show the thermal management of a power MOSFET cooled by a natural convection heat sink and operating with 100W power pulses. The power is supplied with a pulse width of 500ms and a duty cycle of 50%. The study will show how to design and select the right cooling solution for this application and the use of electrical network modelling.

2 Problem description

A single IXYS IXFB38N100Q2 power MOSFET will be used in this paper.

General inputs are as follows:

1. The average dissipated power of the MOSFET is 50W, but the pulsed power has an amplitude of 100W, pulse width of 500ms and a duty cycle of 50%.
2. Ambient temperature is 40°C.

The thermal management of the MOSFET arises some questions:

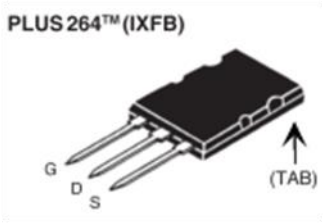
1. How to select the right heat sink?
2. Is selecting the heat sink for average power good enough?
3. What will the junction temperature be under transient operation?

3 Input data

The first step in the thermal analysis is to gather all important input data about the component, its operation and the environmental conditions. The environmental details are as follows: a 40°C ambient temperature and no flow obstructions for the heat sink. The rest of the input data is shown in Table 1, Figure 1 and Figure 2.

Table 1: IXFB38N100Q2 Package Details

Power MOSFET	IXFB38N100Q2	Package	PLUS 264™
Mounting force, *f*	30 to 120 N	Package size	0.76” x 1.007” x 0.185” = 19.3 x 25.6 x 4.7 mm
Weight	10 grams	Package thermal resistance at 500 ms pulse width, $R_{TH\text{-}jc}$	0.13 K/W
Maximum junction temperature	150 °C	Package thermal resistance at 1000 ms pulse width, $R_{TH\text{-}jc}$	0.15 K/W



SYM	INCHES	
	MIN	MAX
A	.185	.209
A1	.102	.118
b	.037	.055
b1	.087	.102
b2	.110	.126
c	.017	.029
D	1.007	1.047
E	.760	.799
e	.215 BSC	
L	.779	.842
L1	.087	.102
Q	.240	.256
Q1	.330	.346
ØR	.155	.187
ØR1	.085	.093

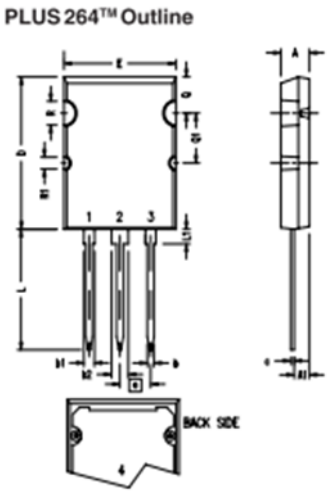


Figure 1: PLUS 264 Package Data

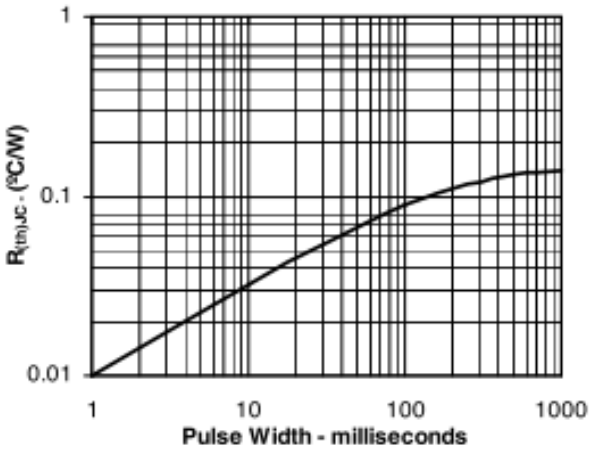


Figure 2: IXFB38N100Q2 Maximum Transient Thermal Resistance

Figure 2 shows that the thermal resistance between junction and case is affected by the pulse width.

4 Calculations

This section will go through steps leading to the initial selection of the cooling solution for the FET. This will include the selection of the interface material and heat sink as well as discussing the mounting pressure. A thermal resistance diagram for the problem is shown in Figure 3.

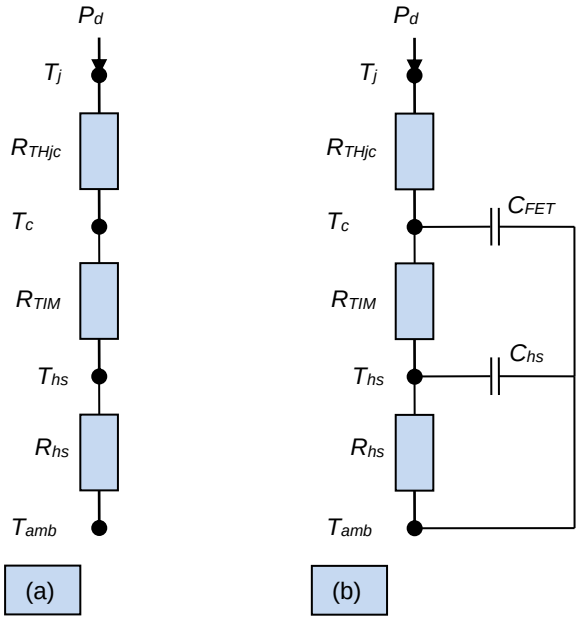


Figure 3: Thermal resistance diagram steady state (a) and transient (b) from FET junction to ambient.

4.1 Confidence Level Factor Calculation

A confidence level factor (CLF) is used to build in a safety factor due to the assumptions, simplifications and errors in the calculation and or measurement method. The confidence level factor depends on how the solution was obtained. The confidence level factors are given below with corresponding method used:

- Analytical: 80%
- Simulation: 85% to 90%
- Experimental: 90%

If is decided that the confidence level factor to be used is 85%. This is applied in equation (1).

$$\frac{T_{j,calc} - T_{ref}}{T_{j,\max} - T_{ref}} \leq 0.85 \qquad (1)$$

The reference temperature for the calculation is ambient temperature, which is 40 °C. The junction condition temperature, $T_{j,max}$, is the maximum junction temperature specified by the manufacturer. Equation (1) can be rewritten to calculate the maximum junction temperature for the calculations to be conducted, as shown in equation (2).

$$T_{j,calc} \leq T_{ref} + 0.85 \times \left(T_{j,\max} - T_{ref}\right) \qquad (2)$$

By using a factor of 85% the junction temperature for this device should stay below 134°C instead of the maximum spec value of 150°C, as shown in equation (3).

$$T_{j,calc} \le 40 + 0.85 \times (150 - 40) = 133.5\,°C \quad (3)$$

4.2 Select Interface Material

A typical interface material for this application is for instance the Tgard™ 210. Tgard™ 210 is a thermally conductive, electrically insulating (6000 V) thermal interface pad. The datasheet states an interface impedance of 1.17 °C-cm²/W (689kPa/100psi)

$$R_{TIM} = {h'}/{A} \quad (3)$$

Based on the PLUS 264™ package dimensions the theoretical interface resistance is:

$$R_{TIM,1} = {1.17}/{1.93 \times 2.56} = 0.23\,K/W \quad (4)$$

Based on the heat slug area within the package theoretical interface resistance is:

$$R_{TIM,2} = {1.17}/{1.7 \times 1.95} = 0.35\,K/W \quad (5)$$

It is the author's experience that for thermal interface materials, the material's thermal performance is frequently too optimistic in favour of the manufacturers. Therefore, the author conducted a test to experimentally determine the interface resistance in Optimal Thermal Solution's laboratory.

The measured interface resistance of the FET mounted on a cold plate with a well defined mounting force:

$$R_{TIM,experimental} = 0.42\,K/W \quad (6)$$

$$h'_{experimentally} = 2.08\,°C \cdot cm^2/W$$

This was measured at 689 kPa or 100 psi. The datasheet of the FET specifies a maximum allowed force on the housing of 30-120N, which means maximum used pressure should be below 233kPa or 34 psi. The maximum allowed force on the device is lower than the tested and datasheet given pressure decided is to use a 10% higher value for the interface resistance within the calculations of 1.1*0.42= 0.46 K/W.

4.3 Calculate the required heat sink performance based on average power.

Using the thermal resistance diagram in Figure 3 (a), the junction temperature can be expressed as equation (7). To express the heat sink thermal resistance, equation 7 is modified to equation (10).

$$T_j = T_{amb} + P_d \times \left(R_{THjc} + R_{TIM} + R_{spreading,hs} + R_{hs-air}\right) \quad (7)$$

$$\frac{\left(T_j - T_{amb}\right)}{P_d} = R_{THjc} + R_{TIM} + R_{spreading,hs} + R_{hs-air} \quad (8)$$

$$R_{spreading,hs} + R_{hs-air} = \frac{\left(T_j - T_{amb}\right)}{P_{d,av}} - \left(R_{THjc} + R_{TIM}\right) \quad (9)$$

$$R_{hs} = R_{spreading,hs} + R_{hs-air} \leq \frac{\left(133.5 - 40\right)}{50} - \left(0.14 + 0.46\right) = 1.28\,\text{K/W} \quad (10)$$

A heat sink with the width 130, length 90 and a height of 30 mm, optimized for natural convection, has an expected theoretical thermal resistance of 0.92K/W and the spreading resistance 0.3 K/W. Therefore, the heat sink thermal resistance is 1.28 K/W, as per equation (11).

$$R_{hs} = R_{spreading,hs} + R_{hs-air} = 0.92 + 0.3 = 1.28\,\text{K/W} \quad (11)$$

4.4 Junction temperature at steady state average power

With the input gathered from the previous steps we can calculate the expected junction temperature under average power conditions:

$$T_j = T_{amb} + P_d \times \left(R_{THjc} + R_{TIM} + R_{spreading,hs} + R_{hs-air}\right) \quad (7)$$

$$T_j = 40 + 50 \times \left(0.15 + 0.46 + 0.3 + 0.92\right) = 132\,^{\circ}\text{C} \quad (12)$$

This is within specification with a confidence level of 85%.

4.5 Junction temperature at steady state peak power

Using the peak power of 100W as a steady state value will give the following junction temperature:

$$T_j = T_{amb} + P_d \times \left(R_{THjc} + R_{TIM} + R_{spreading,hs} + R_{hs-air}\right) \quad (7)$$

$$T_j = 40 + 100 \times \left(0.15 + 0.46 + 0.3 + 0.92\right) = 224\,^{\circ}\text{C} \quad (13)$$

This is far above specification. Therefore, a heat sink with a much lower thermal resistance is required. This would mean a much larger heat sink, possibly with a fan. It must be noted that the result implies a 100% duty cycle.

4.6 Junction temperature at pulsed power; pulse 500ms pulse width duty cycle 50%

For the 50% duty cycle, the transient behaviour of the FET will be analyses using a transient electrical equivalent network. The transient electrical circuit of the thermal problem is shown in Figure 3 (b). For the FET, it is assumed that the copper heat slug is mainly responsible for the thermal capacity and not the junction. Therefore, there is no reduction in R_{THjc} is required while the pulse width is 500ms, see Figure 2.

The thermal capacitance of the FET and heat sink is calculated as follows:

$$C = mc_p \tag{14}$$

$$C_{FET} = m_{FET}c_{p,FET} = \rho wLhc_{p,FET} = 8940 \times 0.017 \times 0.0195 \times 0.00163 \times 385 = 1.86\,\text{J/K} \tag{15}$$

$$C_{HS} = m_{AL}c_{p,AL} = 0.27 \times 897 = 242\,\text{J/K} \tag{16}$$

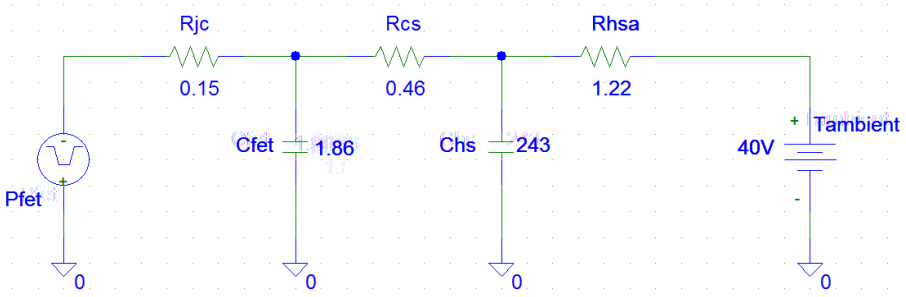


Figure 4: Electrical analogy of the FET on a heat sink.

It is assumed that the dissipated power in the FET has the waveform as shown in Figure 5. The power has a square pulse shape. It is on for 500 ms and thereafter off for an other 500 ms after which the pulse is repeated indefinitely. Since the times are equal, this means a 50% duty cycle.

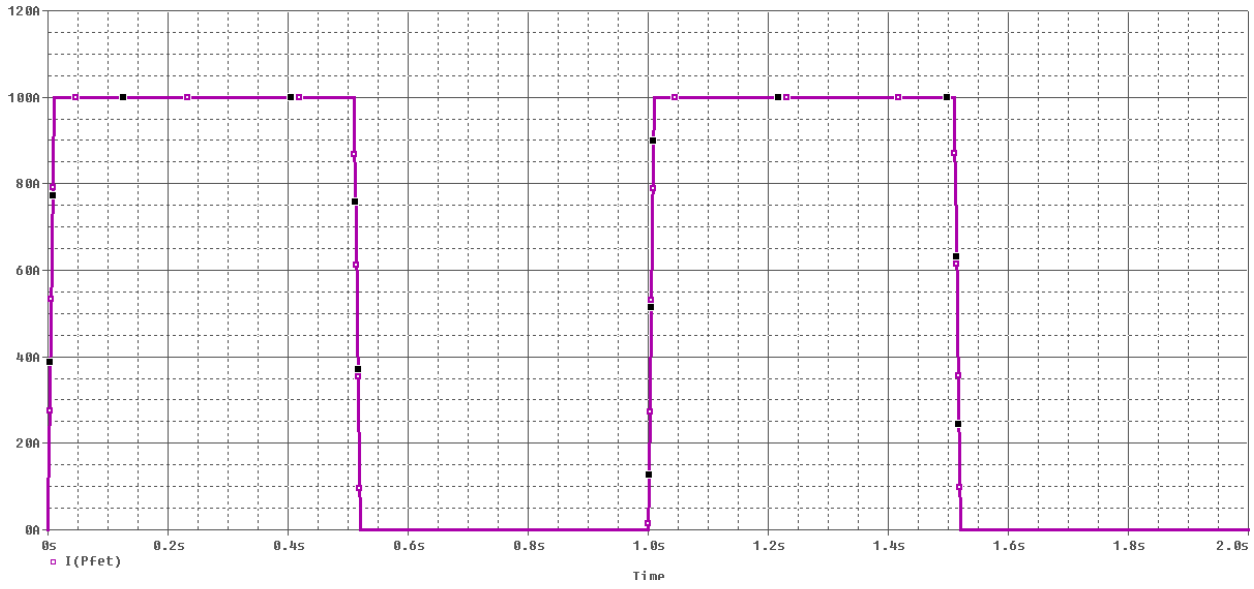


Figure 5: Dissipated power in the FET for the first two seconds.

The temperature response of the FET junction and the heat sink for the first 10 seconds are shown in Figure 6. Figure 6 shows the slow temperature response of the heat sink while the FET junction increases rapidly. This is because the heat sink has a much higher thermal capacitance than the FET. The junction already reaches peaks of 85°C while the heat base was maximum 42°C, which is 2°C higher than the ambient.

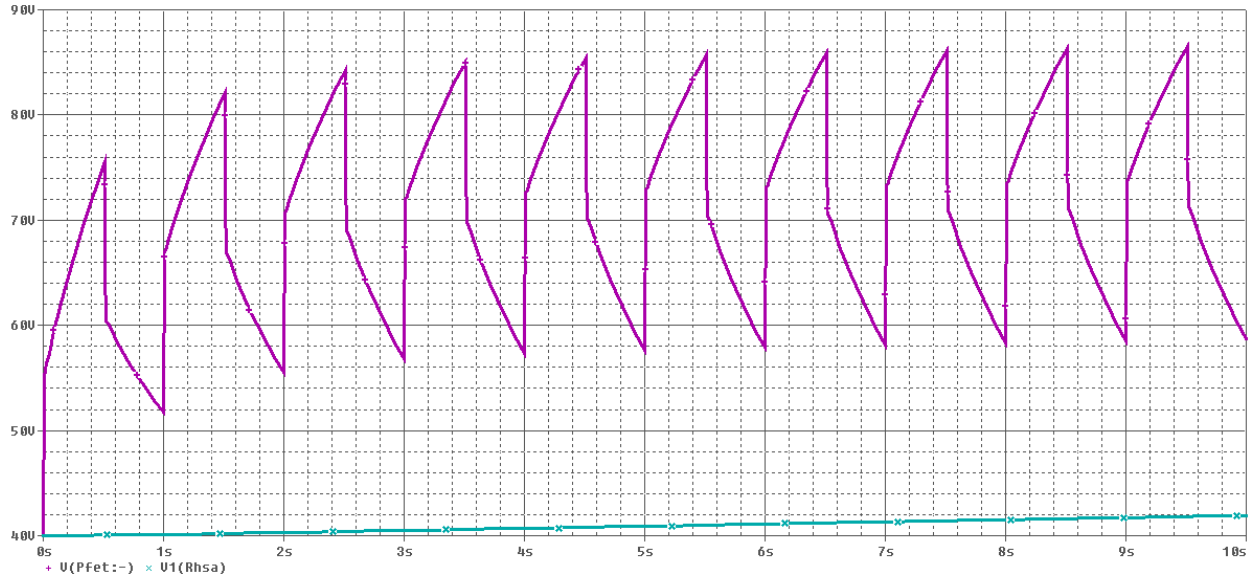


Figure 6: Temperature response of FET junction and heat sink base in the first 10 seconds for 100 ms, 50% duty cycle.

Figure 7 shows that after 10 minutes (or 600 seconds), the temperatures have not stabilized.

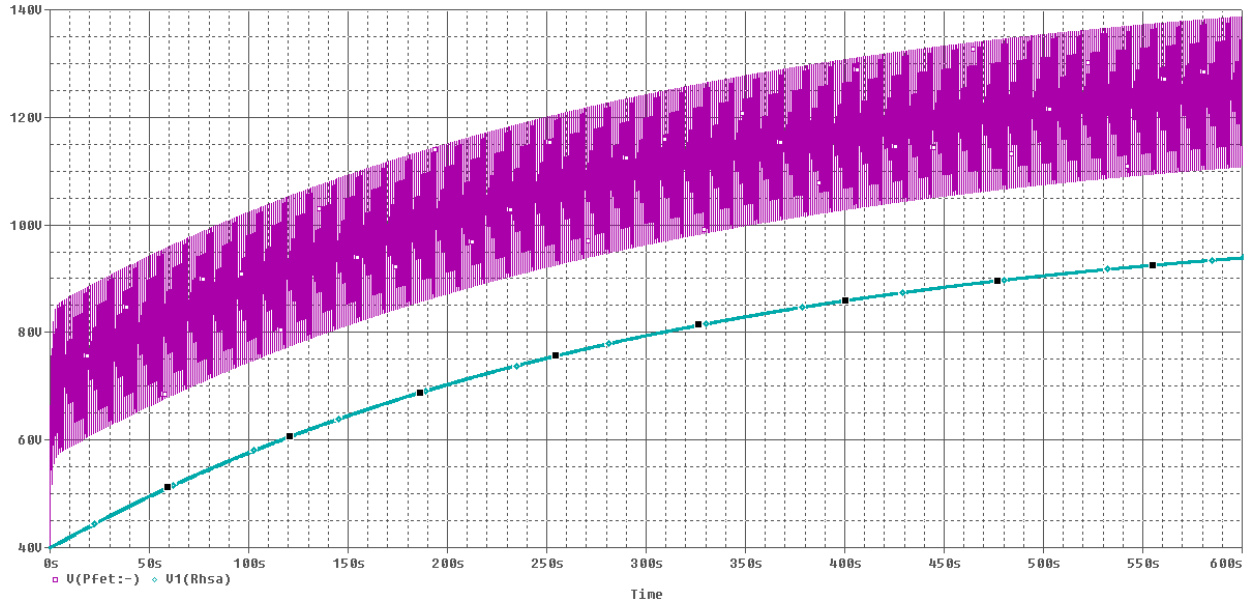


Figure 7: Temperature response of FET junction and heat sink base in the first 10 seconds for 100 ms, 50% duty cycle.

And after 2400 seconds the temperatures become stable. The heat sink base reaches a temperature of 102°C and while the FET's junction reaches 147°C.

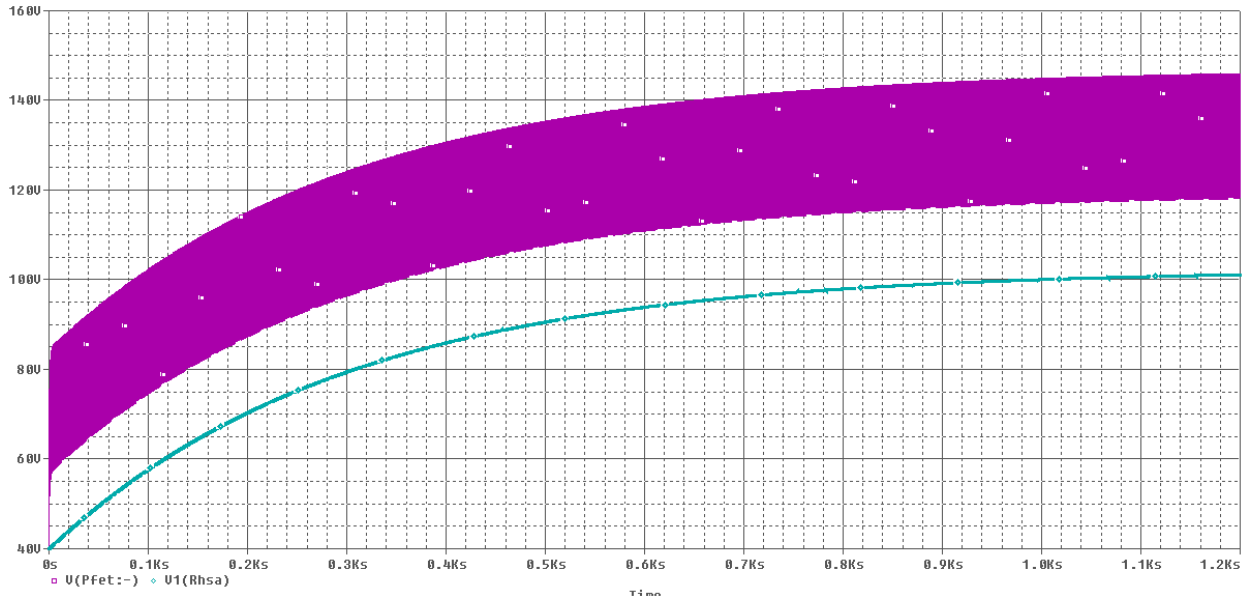


Figure 8: Temperature response of FET junction and heat sink base in the first 1200 seconds for 100 ms, 50% duty cycle.

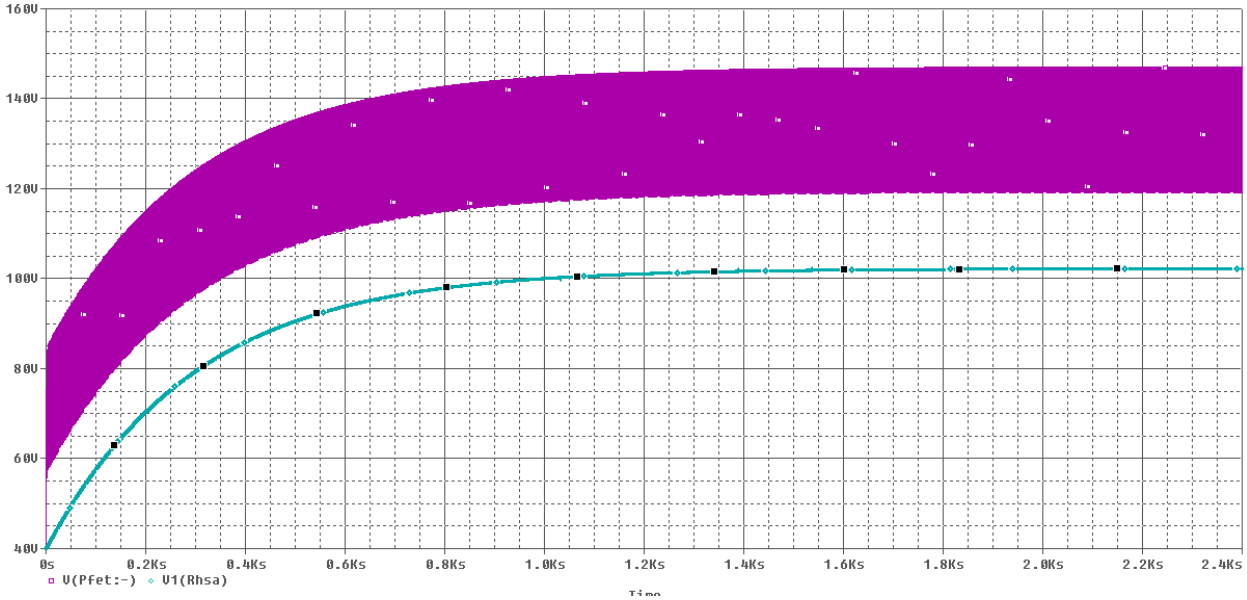


Figure 9: Temperature response of FET junction and heat sink base in the first 2400 seconds for 100 ms, 50% duty cycle.

4.7 Junction temperature effect of pulse width

This section will detail the temperature response of the FET if the pulse width is changed. The pulse widths to be investigated are 1000 ms and 100 ms with a duty cycle of 50%. Using Figure 2, the junction to case thermal resistance for a 100 ms pulse with is 0.095 K/W. In the transient response for the 100 ms pulse width and 50% duty cycle is shown in Figure 10. Figure 10 shows that the maximum heat sink temperature is 107°C while the maximum junction is 143°C. In this case, the heat sink becomes 5°C hotter and the junction 4°C colder due to the change in duty cycle.

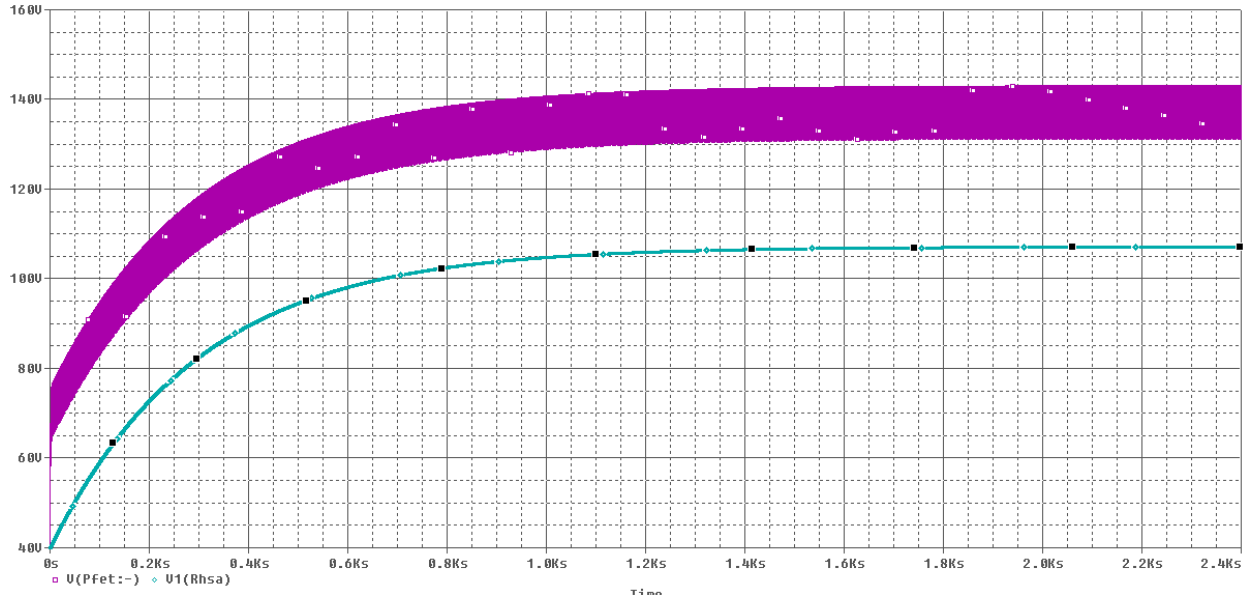


Figure 10: Temperature response of FET junction and heat sink base in the first 2400 seconds, pulse width 100ms@ duty cycle 50%

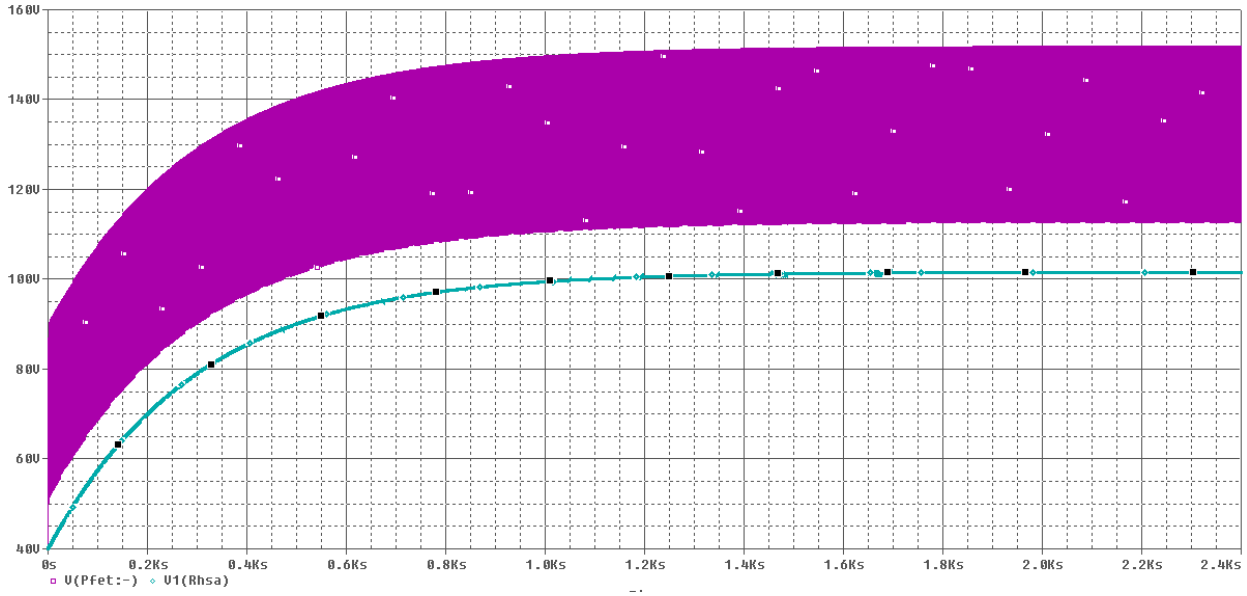


Figure 11: Temperature response of FET junction and heat sink base in first 2400 seconds and pulse width of 1000ms at a duty cycle 50%.

For a 1000 ms pulse width, Figure 11 shows that the effect on the heat sink base is unchanged at 102°C. But the temperature changes and maximum reached in the junction is much more, FET junction reached is 152 °C max, which is 5°C hotter than the case with a pulse width of 500ms. Table 2 shows an overview of the results.

Table 2: Overview results

Peak power	Pulse width	Duty cycle	T_{amb}	$T_{hs,base}$	T_j	$T_{j,max}$	$T_{j,max}$ CLF 85%
[W]	[ms]	[%]	[°C]	[°C]	[°C]	[°C]	[°C]
100	100	50%	40	107	143	150	134
100	500	50%	40	102	147	150	134
100	1000	50%	40	102	152	150	134
100	NA	100%	40	161	222	150	134
50	NA	100%	40	102	132	150	134

Table 2 shows that in all but the 50W/100% duty cycle, the FET junction temperature exceeds the CLF temperature of 134 °C. This shows that in order to keep the current electrical requirements, a better cooling solution needs to be selected. A better cooling solution can be achieved by using a heat sink with a lower thermal resistance and or a better thermal interface material. This will be discussed in section 5.

5 Solution

This section will detail the steps that can be taken in order to get the FET's junction temperature below the CLF temperature of 134°C. The steps to be taken are as follows:

1. Determine the improvement needed to achieve the desired junction temperature.
2. Evaluate the interface material and select an alternative.
3. Select a heat sink with a lower thermal resistance.

In Table 2, it is shown that at 500 ms, the FET junction temperature is 147°C. This is 13 °C above the CLF temperature of 134 °C. Therefore, the combination of the thermal interface material and heat sink needs to be improved by 13 °C. In thermal resistance terms, this mean an improvement of 13 °C with an average dissipation of 50 W, which is 0.26 K/W improvement.

This current cooling solution resistance is:

$$R_{c-amb} = R_{TIM} + R_{spreading} + R_{hs}$$

$$R_{c-amb} = 0.46 + 0.3 + 0.92 = 1.68\,\text{K/W}$$

The new cooling solution needs to have a value of:

$$R_{c-amb} = 1.68 - 0.26 = 1.42\,\text{K/W}$$

5.1 Selecting of a better TIM material

The currently used TIM material (Tgard™ 210) has a thermal impedance value of 1.17 °C·cm²/W specified in the data sheet. When measured, it was found that thermal impedance was 2.08 °C·cm²/W. The Tgard™ 210 can be replaced by phased change materials or thermal paste. The aforementioned materials are not electrically insulating, but this is not a problem with the current application. Typical thermal impedance values are between 0.5 and 1 °C·cm²/W. For the purposes of this white paper, we will assume a value of 0.75 °C·cm²/W.

Based on the PLUS 264™ package dimensions the theoretical interface resistance is:

$$R_{TIM} = {}^{0.75}\!\diagup_{1.93 \times 2.56} = 0.15\,\text{K/W}$$

Based on the heat slug area within the package theoretical interface resistance is:

$$R_{TIM2} = {}^{0.75}\!\diagup_{1.7 \times 1.95} = 0.23\,\text{K/W}$$

It is decided that the thermal resistance value based on the heat slug area will be used in the calculations. The difference between the previously used interface resistance of 0.42 K/W and the new interface resistance of 0.23 K/W, is 0.19 K/W. The difference is nearly the improvement required, which is 0.26 K/W. Therefore, a small additional improvement is needed from the heat sink, namely 0.26 K/W – 0.19 K/W = 0.07 K/W.

5.2 Selecting/ designing a better heat sink

The currently used heat sink, as selected in section 4.3, has a thermal resistance of 1.22 K/W. In section 5.1, the heat sink needs to be improved by 0.07 K/W. The required improvement can be achieved by adding an additional fin or making the heat sink slightly longer if a standard extrusion was selected.

The interface material can not be changed, then the improvement required needs to come entirely from the heat sink thermal performance. Therefore, a heat sink needs to be selected or designed which has a thermal resistance of 0.96 K/W. This can be achieved by using a heat sink with a width of 130 mm, length of 90 mm and a height of 30 mm, which is 77% larger in volume than the currently used heat sink. The new design heat sink has a weight of 489 g, which is also 81% heavier than the first heat sink. In general, this would mean that the new design heat sink will also be more expensive and will result in a heavier product.

5.3 Check of the improved design

To check the improved design, the transient response of the cooling solution will be modeled in PSpice. The cooling solution will consist of new interface material as well as the improved original design. The schematic is shown in Figure 12 and its transient response is shown in Figure 13. The maximum junction reaches now 134°C max and is within now specification.

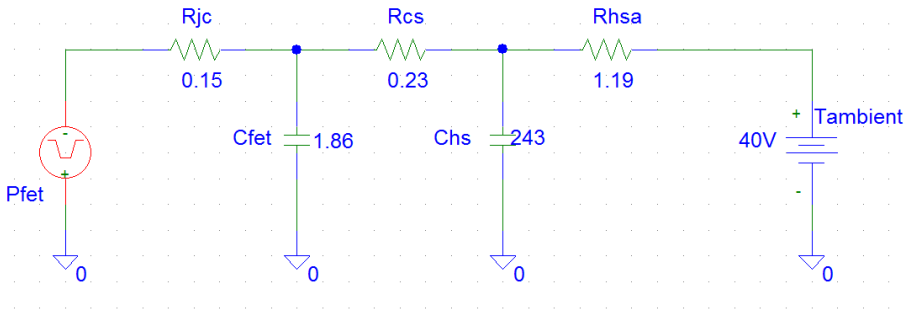


Figure 12: Schematic of improved design

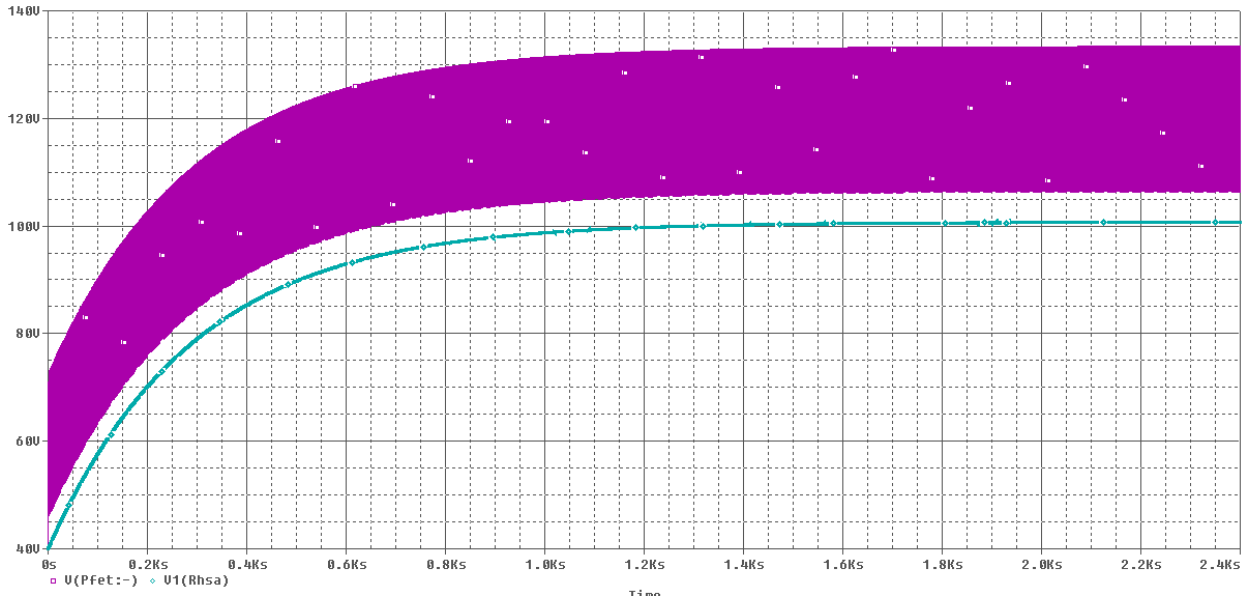


Figure 13: Temperature response of the improved design, pulse width 500ms@ duty cycle 50%.

A steady state simulation was conducted using improved heat sink design. The calculations show a heat sink base temperature under the FET of 102°C. The simulation has a 93°C heat sink base temperature, which is slightly lower than the calculation. This difference between the simulation and calculation is acceptable. The surface temperature plot of the heat sink is shown in Figure 14. A final check needs to done by conducting a test on junction level.

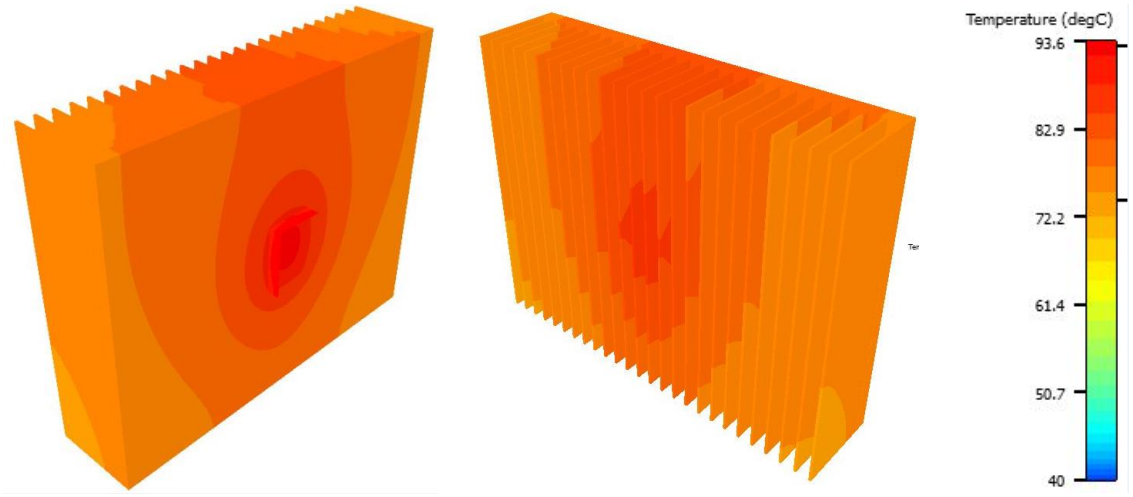


Figure 14: The surface temperature plot of the heat sink generated by conducting a steady state CFD simulation of the problem.

6 Conclusion

A power MOSFET used with pulsed power dissipation can fail if the thermal design is only based on average power dissipation. This study shows the thermal management for a power MOSFET cooled by a natural convection heat sink and operating with 100W power pulses. The power is supplied with a pulse width of 500ms and a duty cycle of 50%. The study will show how to design and select the right cooling solution for this application and the use of electrical network modelling.

This article has shown that the cooling solution for a pulsed powered MOSFET can not be selected based on the average power dissipation. The maximum junction temperature reached depends on the pulse width, peak power and duty cycle. Detailed transient analyses and experiments are required to come to an optimal thermal design. The study also showed that a detailed analyses and evaluation of the problem will give insight in the problem areas and how to solve it in the most optimal way with the lowest cost.